Thoughts on the Significance of IBM's EUV Benchmark

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Since I posted in last week's *EUVL Focus* blog the news of IBM's EUV benchmark with the NXE3300B scanner at the EUV Center of Excellence in Albany, this news has received lots of attention, as it is a significant achievement. I have also received some questions and comments. I believe most of them come from a lack of familiarity with leading edge tool development and with EUV Lithography itself, which is a rather narrow area of specialization. As I tend to give long answers and reviews (because I believe details are important) in this blog I will give first give a "short-short answer" followed by a "short answer." I will leave the "long answer" regarding the significance of this announcement for future blogs.

Short-short answer:

There is no change in the significance of what was reported last week. ASML and IBM reconfirmed the benchmarking in press and via social media. In short, 637 wafers per day throughput stands, resulting from the successful upgrade of source power by 100%, to its targeted level of ~43 W. Of course, this is a data point that needs to be confirmed over a longer period and by additional leading edge chip makers, but this was already suggested from the very beginning.

Short Answer:

(1) In the process of benchmarking leading edge tools, the performance of the tool is divided into several sections and each part is validated separately. One can divide an EUVL scanner into the major components of optics, source, mask and resist. All parts, except higher power for EUV light source, have been validated for a long time – with challenges remaining but no showstopper. High source power has remained the #1 issue and a potential showstopper. The ~40 W EUV light sources were deployed but have been working at the lower level of 20 W. The validation at 43 W is a ~100% improvement in source power. The previously reported throughput for an EUVL scanner was 200 wafers per day (WPD), so 637 WPD is over three times

improvement and exceeds ASML' s own expectation of 500 WPD for 2014. One chip maker earlier this year privately told me that ~1000 Wafers per day is acceptable for the selection of EUVL for high volume manufacturing (HVM). Hence, this excitement can be understood. I believe that ASML has moved to WPD as the new unit for the measurement of performance of their EUVL scanner, as this is more meaningful unit to chipmakers than source power, as it directly relates to productivity.

(2) The imaging performance of EUV scanners (CD, CDU, pitch, LER) are a function of scanner design, optics, mask, source and resist. The performance of these parts, except source, has been confirmed for some time now and needs no new validation. The source stability has some effect as well on imaging; hence, the power has to be stable and it is one reason for lower power results from the field. However, the #1 issue for EUV has been the throughput of the EUV scanner, which is directly related to the power of the source, as I mentioned above. Although one will eventually test the imaging performance at higher power levels, it does not make sense to be doing that imaging test (and when you know that part works fine) when you are testing for source power upgrade verification – your main challenge. This is how one benchmarks complex machines. As IBM pointed out, it was an unintended but very exciting result of their benchmark, as the focus was to validate higher source power. Other parts of the scanner and the overall imaging performance have been verified by several chip makers for some time.

(3) The next version of the NXE3300B EUV scanner will be potentially used for patterning at the 7 nm and 5 nm nodes. The resolution of printed images will be increased by either multiple patterning (EUV MP), which has been already demonstrated, or via high NA optics (projects are in progress but no demonstration of a high NA EUV tool has occurred yet). Please see the keynote talks from Toshiba and Intel in the 2014 EUVL Workshop proceedings at www.euvlitho.com to get additional information on these topics.

(4) 20 mJ of dose for a chemically amplified (CAR) resist, to test the throughput of a EUV scanner, is a very decent dose choice and it is backed by ample data. If this benchmark was done for a 5 mJ CAR resist dose, I will question the test as well, as final images will not meet LER requirements. The good news is that due to recent developments in the high sensitivity resists, now 2-5 mJ dose can give us the same resolution and LER, as from 20 mJ or higher dose CAR resists. In the 2014 SPIE AL meeting, there were many papers confirming the performance of these new types of resists. Hence, the triangle of death (sensitivity, LER and resolution) for CAR resists is no longer valid for these new types of resists. The implications of these new resists are very striking – if we can use these new 5 mJ resists – the throughput will be 3-4 x larger than what is reported for 20 mJ resists. I am hoping that these new high sensitivity resists will mature in another year for HVM use.

(5) Some comments in the press have made over the years, hinting that a "leading chip maker" is working on 193 nm multiple mattering (193 MP), the current workhorse, in addition to EUV for the next node of patterning technology. The comments are made as if this is a "negative" implication for EUV. The fact is that every leading chip maker has been looking at both technologies (193 MP and EUV plus EUV MP) for a long time, and will continue to do so until EUV is in production to hedge their risks, and expecting anything else would not be wise. 193 MP extension is costly due to tooling and mask costs, low throughput of overall manufacturing line and lower yields. This choice also puts severe restrictions on what can be printed. EUV relaxes k1 value by turning the wavelength knob in the Rayleigh's resolution criterion and hence the emphasis on EUV.

(6) I will not try to pretend that I understand how the stock market works, but the stock of ASML did jump over 14% in one day with this news of new EUV Benchmark. What some people do not know is that ASML is a winner if the industry chooses EUV/ EUV MP or its competitor of 193 MP. ASML is the only maker of EUVL scanners and the leading maker of scanners used for 193 MP. It is a win-win situation for ASML either way, and few other high tech companies can claim such a strategic advantage.

I hope this explains the significance of the EUV benchmark news. In the longer version of my response, I will explain different sections of the EUV scanner and how and why the throughput of the EUV scanner is related to NA, mask, resist, optics and source performance. In addition to writing this blog, organizing EUV related workshops and consulting work, I also teach, together with two of my colleagues, a short course on EUV Lithography twice a year (during the annual SPIE AL meeting and during the annual EUVL workshop).I also hope that if this topic is of interest, I will see you in the classroom where we all can have further discussions.